Ke Huang

Associate Professor
Department of Electrical and Computer Engineering
San Diego State University
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Research Interests

- VLSI testing, trustworthy ICs
- Computer-aided design of ICs
- Machine learning, data mining
- Intelligent vehicles

Education

Université Grenoble Alpes — Grenoble, France
Ph.D. in Electrical Engineering — November 2011
Thesis Title: Fault modeling and diagnosis for nanometric mixed-signal/RF circuits
Advisors: Salvador Mir, Haralampos-G. Stratigopoulos

Université Grenoble Alpes — Grenoble, France
M.S. in Electrical Engineering — July 2008

Université Grenoble Alpes — Grenoble, France
B.S. in Electrical Engineering — July 2006

Professional Positions

San Diego State University — San Diego, CA, USA
Associate Professor, Department of Electrical and Computer Engineering — 2020-Present

San Diego State University — San Diego, CA, USA
Assistant Professor, Department of Electrical and Computer Engineering — 2014-2020

The University of Texas at Dallas — Richardson, TX, USA
Post-Doctoral Research Associate, Department of Electrical Engineering — 2012-2014

French National Centre for Scientific Research (CNRS) — Grenoble, France
Research Assistant — 2008-2011

Teaching

- San Diego State University
  - EE 671 - VLSI Testing, Fall 2017-23, Spring 2017-22
  - COMPE 572 - VLSI Circuit Design, Fall 2015
  - EE 530 - Analog Integrated Circuit Design, Spring 2023-24
  - COMPE 470L - Digital Logic Laboratory, Fall 2021-23, Spring 2022-24
  - COMPE 375 - Embedded System Programming, Spring 2019-21
  - COMPE 270 - Digital Systems, Fall 2014-23, Spring 2015-24

Honors and Awards

- Funding
  - "An Eco-Driving System for Connected Automated Vehicles based on Multi-Objective Trajectory Optimization", California State University Transportation Consortium, Single PI, $74,877, 05/2019 - 04/2020.
  - "Optimization of Semiconductor Manufacturing Process Based on Data Mining", Innophase Inc., Single PI, $27,706, 02/2019 - 06/2019.
  - "Volitional Movement Intention Decoding based on Low-Power On-Chip Intelligence", NSF Center for Sensorimotor Neural Engineering (CSNE), Single PI, $20,000, 09/2015 - 09/2016.
  - "Qualcomm Support for Dr. Huang's Research", Qualcomm Inc., Single PI, $30,000, 06/2015 - 09/2015.

- Academic Awards
  - Best Presentation Award, International Conference on Artificial Intelligence and Big Data 2023 (ICAIBD'23)
  - Best Paper Award, IEEE VLSI Test Symposium 2015 (VTS'15)
  - Best Paper Award, Design, Automation and Test in Europe conference 2013 (DATE'13)
  - 2nd Place Winner, IEEE Computer Society Test Technology Technical Council (TTTC) E. J. McCluskey Best Doctoral Thesis Award 2013.
  - Ph.D. Fellowship from French Ministry of National Education

Publications

Book Chapters:

[B1] A. Elfadel, D. Bonning and X. Li (Editors), *Machine Learning in VLSI Computer-Aided Design*, Springer, 2018 (N. Kupp, **K. Huang**, A. Ahmadi, C. Xanthopoulos, and Y. Makris, "Gaussian Process-Based Wafer-Level Correlation Modeling and its Applications").

[B2] T. Hokimoto (Editors), *Advances in Statistical Methodologies and Their Application to Real Problems*, InTech, 2017 (M. Agrawal, S. Vidyashankar, and **K. Huang**, “On Decoding Brain Electrocorticography Data for Volitional Movement Intention Prediction: Theory and On-Chip Implementation”).

Peer-Reviewed Journal Papers:

[J1] X. Zhang, M. Samragh, S. Hussain, **K. Huang**, and F. Koushanfar, “Scalable binary neural network applications in oblivious inference,” *ACM Transactions on Embedded Computing Systems*. (in press)

[J2] **K. Huang**, Y. Liu, N. Korolija, J. Carulli, and Y. Makris, “Statistical methods for detecting recycled electronics: from ICs to PCBs and beyond,” *IEEE Design & Test*, vol. 41, no. 2, pp. 15-22, 2024.

[J3] H. Chen, X. Zhang, **K. Huang**, and F. Koushanfar, “AdaTest: reinforcement learning and adaptive sampling for on-chip hardware Trojan detection,” *ACM Transactions on Embedded Computing Systems*, vol. 22, no. 2, pp. 1-23, 2023.

[J4] D. Ma, X. Zhang, **K. Huang**, Y. Jiang, W. Chang, and X. Jiao, “DEVoT: dynamic delay modeling of functional units under voltage and temperature variations,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 4, pp. 827-839, 2022.

[J5] X. Yang, **K. Huang**, Z. Zhang, Z. Zhang, and F. Lin, “Eco-driving system for connected automated vehicles: multi-objective trajectory optimization,” *IEEE Transactions on Intelligent Transportation Systems (TITS)*, vol. 22, no. 12, pp. 7837-7849, 2021.

[J6] **K. Huang**, X. Zhang, and N. Karimi, “Real-time prediction for IC aging based on machine learning,” *IEEE Transactions on Instrumentation & Measurement*, vol. 68, no. 12, pp. 4756-4764, 2019.

[J7] P. Kansara, S. Reddy, L. Abdallah, **K. Huang**, “Dynamic analog/RF alternate test strategies based on on-chip learning,” *Journal of Electronic Testing: Theory & Applications (JETTA), Springer*, vol. 34, no. 3, pp. 337-349, 2018.

[J8] **K. Huang**, X. Yang, Y. Lu, C. Mi, and P. Kondlapudi, “Ecological driving system for connected/automated vehicle using a two-stage control hierarchy,” *IEEE Transactions on Intelligent Transportation Systems (TITS)*, vol. 19, no. 7, pp. 2373-2384, 2018.

[J9] A. Ahmadi, H.-G. Stratigopoulos, **K. Huang**, A. Nahar, B. Orr, M. Pas, J. M Carulli, and Y. Makris, “Yield forecasting across semiconductor fabrication plants and design generations,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 12, pp. 2120-2133, 2017.

[J10] **K. Huang**, J. Wen, and J. Willmore, “Test-suite based analog/RF test time reduction using canonical correlation,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 12, pp. 2143-2147, 2016.

[J11] **K. Huang**, Y. Liu, N. Korolija, J. Carulli, and Y. Makris, “Recycled IC detection based on statistical methods,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 6, pp. 947-960, 2015.

[J12] **K. Huang**, N. Kupp, C. Xanthopoulos, J. Carulli, and Y. Makris, “Low-cost analog/RF IC testing through combined intra- and inter-die correlation models,” *IEEE Design & Test*, vol. 32, no. 1, pp. 53-60, 2015.

[J13] U. Guin, **K. Huang**, D. DiMase, J. Carulli, M. Tehranipoor, and Y. Makris, “Counterfeit integrated circuits: a rising threat in the global semiconductor supply chain,” *Proceedings of the IEEE*, vol. 102, no. 8, pp. 1207-1228, 2014.

[J14] **K. Huang**, H.-G. Stratigopoulos, S. Mir, C. Hora, Y. Xing and B. Kruseman, “Diagnosis of local spot defects in analog circuits,” *IEEE Transactions on Instrumentation and Measurement (TIM)*, vol. 61, no. 10, pp. 2701-2712, 2012.

Peer-Reviewed Conference Papers:

[C1] Z. Ghodsi, M. Javaheripi, N. Sheybani, X. Zhang, **K. Huang**, and F. Koushanfar, “zPROBE: zero peek robustness checks for federated learning”, in *Proc. of IEEE/CVF International Conference on Computer Vision (ICCV)*, 2023, pp. 4860-4870.

[C2] **K. Huang** and L. Abdallah, “Analog/RF circuit aging prediction based on on-chip machine learning”, in *Proc. of International Conference on Artificial Intelligence and Big Data (ICAIBD)*, 2023, pp. 294-298.

[C3] **K. Huang**, Md T. H. Anik, X. Zhang, and N. Karimi, “Real-time IC aging prediction via on-chip sensors”, in *Proc. of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2021, pp. 1-6.

[C4] M. Samragh, S. Hussain, X. Zhang, **K. Huang**, and F. Koushanfar, “On the application of binary neural networks in oblivious inference”, in *Proc. of CVPR 1st Workshop on Binary Networks for Computer Vision*, 2021, pp. 1-10.

[C5] F. Lin, A. Ahmadi, K. Sekar, Y. Pan, and **K. Huang**, “IC layout weak point quality evaluation based on statistical methods”, in *Proc. of IEEE VLSI Test Symposium (VTS)*, 2018, pp. 1-6.

[C6] N. Karimi and **K. Huang**, “Prognosis of NBTI aging using a machine learning scheme”, in *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Storrs, CT, USA, 2016, pp. 1-4.

[C7] M. Agrawal, S. Vidyashankar, and **K. Huang**, “On-chip implementation of ECoG signal data decoding in brain-computer interface”, in *Proc. of International Mixed-Signal Testing Workshop (IMSTW)*, Sant Feliu de Guixols, Spain, 2016, pp. 1-6.

[C8] Y. Lu, K. Subramani, H. Huang, N. Kupp, **K. Huang**, and Y. Makris, “A comparative study of one-shot statistical calibration methods for analog/RF ICs”, in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, 2015, Paper 21.3 (Acceptance rate 30%).

[C9] Y. Liu, G. Volanis, **K. Huang**, and Y. Makris, “Concurrent hardware Trojan detection in wireless cryptographic ICs”, in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, 2015, Paper 4.1 (Acceptance rate 30%).

[C10] A. Ahmadi, **K. Huang**, A. Nahar, B. Orr, M. Pas, J. Carulli, and Y. Makris, "Yield prognosis for fab-to-fab product migration", in *Proc. of IEEE VLSI Test Symposium (VTS)*, Napa, CA, USA, 2015, pp. 1-6 (Best paper award).

[C11] C. Xanthopoulos, **K. Huang**, A. Poonawala, A. Nahar, B. Orr, J. Carulli, and Y. Makris, "IC laser trimming speed-up through wafer-level spatial correlation modeling", in *Proc. of IEEE International Test Conference (ITC)*, Seattle, WA, USA, 2014, Paper 19.2 (Acceptance rate 25%).

[C12] A. Ahmadi, **K. Huang**, S. Natarajan, J. Carulli, and Y. Makris, "Spatio-temporal wafer-level correlation modeling with progressive sampling: a pathway to HVM yield estimation", in *Proc. of IEEE International Test Conference (ITC)*, Seattle, WA, USA, 2014, Paper 18.1 (Acceptance rate 25%).

[C13] Y. Liu, **K. Huang**, and Y. Makris, "Hardware Trojan detection through golden chip-free statistical side channel fingerprinting", in *Proc. of Design Automation Conference (DAC)*, San Francisco, CA, USA, June 2014, pp. 1-6 (Acceptance rate 23%).

[C14] **K. Huang**, J. Carulli, and Y. Makris, "Counterfeit electronics: a rising threat in the semiconductor manufacturing industry", in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, September 2013, Paper L3.4 (Acceptance rate 30%).

[C15] **K. Huang**, H.-G. Stratigopoulos, and S. Mir, "Fault modeling and diagnosis for nanometric analog/mixed-signal/RF circuits," in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, September 2013, Paper PTF3 (Acceptance rate 30%).

[C16] **K. Huang**, N. Kupp, J. Carulli, and Y. Makris, "Process monitoring through wafer-level spatial variation decomposition," in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, September 2013, Paper 5.3 (Acceptance rate 30%).

[C17] O. Sinanoglu, N. Karimi, J. Rajendran, R. Karri, Y. Jin, **K. Huang**, and Y. Makris, "Reconciling the IC test and security dichotomy," in *Proc. of IEEE European Test Symposium (ETS)*, Avignon, France, May 2013, pp. 1-6 (Acceptance rate 30%).

[C18] **K. Huang**, N. Kupp, J. Carulli, and Y. Makris, "On combining alternate test with spatial correlation modeling in analog/RF ICs," in *Proc. of IEEE European Test Symposium (ETS)*, Avignon, France, May 2013, pp. 1-6 (Acceptance rate 30%).

[C19] **K. Huang**, H.-G. Stratigopoulos, L. Abdallah, S. Mir, and A. Bounceur, "Multivariate statistical techniques for analog parametric test metrics estimation," in *Proc. of IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS)*, Abu Dhabi, UAE, March 2013, pp. 6-11.

[C20] **K. Huang**, N. Kupp, J. Carulli, and Y. Makris, "Handling discontinuous effects in modeling spatial correlation of wafer-level analog/RF tests," in *Proc. of Design, Automation and Test in Europe conference (DATE)*, Grenoble, France, March 2013, pp. 553-558 (Best paper award) (Acceptance rate 24.8%).

[C21] K. Beznia, A. Bounceur, L. Abdallah, **K. Huang**, S. Mir, and R. Euler, "Accurate estimation of analog test metrics with extreme circuits," in *Proc. of IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Seville, Spain, December 2012, pp. 272-275.

[C22] N. Kupp, **K. Huang**, J. Carulli, and Y. Makris,"Spatial estimation of wafer measurement parameters using Gaussian process models", in *Proc. of IEEE International Test Conference (ITC)*, Anaheim, CA, USA, November 2012, pp. 1-8 (Acceptance rate 30%).

[C23] N. Kupp, **K. Huang**, J. Carulli, and Y. Makris, "Spatial correlation modeling for probe test cost reduction", in *Proc. of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, USA, November 2012, pp. 23-29 (Acceptance rate 24.3%).

[C24] **K. Huang**, J. Carulli, and Y. Makris, "Parametric counterfeit IC detection via support vector machines", in *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Austin, TX, USA, October 2012, pp. 7-12.

[C25] **K. Huang**, H.-G. Stratigopoulos, and S. Mir, "Bayesian fault diagnosis of RF circuits using nonparametric density estimation," in *Proc. of IEEE Asian Test Symposium (ATS)*, Shanghai, China, December 2010, pp. 295-298.

[C26] **K. Huang**, H.-G. Stratigopoulos, and S. Mir, "Fault diagnosis of analog circuits based on machine learning," in *Proc. of Design, Automation and Test in Europe conference (DATE)*, Dresden, Germany, March 2010, pp. 1761-1766 (Acceptance rate 24.8%).

Professional Service

- Guest Editor
  - Journal of Electronic Testing: Theory and Applications (JETTA), Springer, Special Issue on Analog, Mixed-Signal and RF Testing 2018
- General Chair
  - IEEE International Workshop on Test and Validation of High Speed Analog Circuits 2018 (TVHSAC'18)
- Program Chair
  - International Mixed-Signal Testing Workshop 2017 (IMSTW'17)
- Finance Chair
  - IEEE VLSI Test Symposium 2022-23 (VTS' 22-23)
- Registration Chair
  - IEEE VLSI Test Symposium 2019-21 (VTS' 19-21)
- Audio/Visual Chair
  - IEEE VLSI Test Symposium 2017-18 (VTS' 17-18)
- Publicity Chair
  - IEEE International Workshop on Test and Validation of High Speed Analog Circuits 2015 (TVHSAC'15)
- Publication Chair
  - International Mixed-Signal Testing Workshop 2016-15 (IMSTW'15-16)

- Program Committee Member
  - International Conference on Artificial Intelligence and Big Data 2022-23 (ICAIBD'22-23)
  - IEEE International Test Conference 2018-15 (ITC'15-18)
  - IEEE Asian Test Symposium 2014 (ATS'14)
- Reviewer
  - IEEE Transactions on Circuits and Systems I (TCAS-I)
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
  - IEEE Transactions on Instrumentation and Measurement (TIM)
  - IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
  - ACM Transactions on Design Automation of Electronic Systems (TODAES)
  - Circuits, Systems and Signal Processing (CSSP)
  - Journal of Electronic Testing: Theory and Applications (JETTA)

Professional Associations

- IEEE Senior Member