Course Title: COMPE470L – Digital Logic Laboratory

Course Description

Course title: Digital Logic Laboratory

Course number: COMPE470L

Credit: 1 Unit

Course description: Hands-on experience in characterization and application of standard digital integrated circuit devices.

Mode of delivery: In-Person Laboratory Sessions

Prerequisite: COMPE470, EE330L

Instructor Contact Information and Office Hours

Instructor's name: Ke Huang, Lana Pantskalashvili

Instructor's email: khuang@sdsu.edu, lpantskalashvi0014@sdsu.edu

Office hours: Tuesday, Thursday: 3:30PM-4:30PM

Student Learning Outcomes (SLO)

1. Discover good lab practices, basic laboratory measurement techniques, and safety rules.
2. Utilize test bench files to simulate/analyze the digital design at both behavioral model level and post-synthesized model level using simulation and hardware test.
3. Discover basic Digital Logic design and debugging techniques.
4. Discover the operation and usage of test and measurement instruments (Oscilloscope, logic analyzer).
5. Design and model both combinational and synchronous sequential logic circuits including finite state machines (FSM), arithmetic logic, data/control path using Verilog HDL.
6. Utilize a computer aided FPGA design tool to model digital design using Verilog HDL for simulation, synthesis and timing analysis of digital systems targeting an FPGA.
7. Discover download and reconfiguration of FPGA with the bit file generated after synthesis and verified.
8. Record experimental data and write laboratory reports.

Student Accommodations

For Students with Disabilities:

If you are a student with a disability and believe you will need accommodations for this class, it is your responsibility to contact Student Disability Services at (619) 594-6473. To avoid any delay in the receipt of your accommodations, you should contact Student Disability Services as soon as possible. Please note that accommodations are not retroactive, and that I cannot provide accommodations based upon disability until I have received an accommodation letter from Student Disability Services. Your cooperation is appreciated.

Textbooks and References

- J. F. Wakerly, *Digital Design: Principles and Practices*, Prentice Hall Digital Systems, 4th Edition, 2005. - Instructor Notes
- FPGA reference materials
- More information on advanced digital design projects can be found at here
- Relevant information on hardware acceleration for AI can be found at here

Lab Resources

- E-207 Lab with PCs, Oscilloscopes, logic analyzers and FPGA boards

Schedule

Week	Lab Schedule	Due
1	Lab 1	
2	Lab 2	Lab 1 Report
3	Lab 3	Lab 2 Report
4	Lab 4	Lab 3 Report
5	Lab 4	
6	Lab 5	Lab 4 Report
7	Lab 5	Project Proposal
8	Lab 6	Lab 5 Report
9	Lab 6	
10	Lab 6	
11	Lab 6	
12	Final Project	Lab 6 Report
13	Final Project	
14	Final Project	
15	Final Project	Final Project Report

Grading Policies

You will be graded in this course as follows:

Lab assignment	Percentage
Lab 1 demo	5%
Lab 1 report	5%
Lab 2 demo	5%
Lab 2 report	5%
Lab 3 demo	5%
Lab 3 report	5%
Lab 4 demo	5%
Lab 4 report	5%
Lab 5 demo	10%
Lab 5 report	10%
Lab 6 demo	10%
Lab 6 report	10%
Final project demo	10%
Final project report	10%

A zero grade will be assigned to the report part if the corresponding demo was not shown to the instructor. The demo for each lab assignment must be shown to the instructor of the session during the designated lab session time, no demo outside the designated lab session time will be considered. The table below shows the aggregated percentage score to letter grade conversion.

Lowest	Highest	Letter
92.00 %	100 %	A
90.00 %	91.99 %	A-
87.00 %	89.99 %	B+
83.00 %	86.99 %	B

Lowest	Highest	Letter
80.00 %	82.99 %	B-
77.00 %	79.99 %	C+
73.00 %	76.99 %	C
70.00 %	72.99 %	C-
67.00 %	69.99 %	D+
63.00 %	66.99 %	D
60.00 %	62.99 %	D-
0.00 %	59.99 %	F

Late Submission Penalty

Lab report due dates are posted under the section “Assignments” in Canvas. Late submissions will result in a reduction of the grade: -10% on the grade for 1 day's late submission, -20% for 2 days, -30% for 3 days, etc. A zero grade will be assigned to the report submitted more than 10 days after the due date.

Please note that if you want to apply for a late submission penalty waiver due to an extraordinary cause, you must prove that your circumstance satisfies any conditions in part 2 of the section "Information on deferred due dates" in the syllabus.

In case you miss a demo due to an extraordinary cause specified in part 2 of the section "Information on deferred due dates", you can show a makeup demo in a later regular lab session. No makeup demo will be considered outside the regular lab session.

Information on Deferred Due Dates

1. Requests to defer lab report due dates will be DENIED if for:

    a) Travel, vacation, or other personal plans; and
    b) Employment reasons.

2. Requests to defer lab report due dates will be considered for the following extraordinary causes:

    a) Physical or mental illness of Student;
    b) Death or serious illness in immediate family;
    c) Automobile accident, mugging, robbery, or similar traumatic experience;

d) Subpoena requiring court appearance on the due date;
e) Childbirth on or immediately preceding the report due date (applies to either parent);
f) Military commitment. Written military orders are required;

If you think your circumstance satisfies any conditions above, please provide me an **official written proof** of your circumstance, so that I can waive the late submission penalty for you.

Student Privacy and Intellectual Property

The confidentiality of student grades and other evaluation of student work is ensured by the use of Canvas system for posting grades for HW/project/midterm/final test. The Canvas online student account system is designed not to disclose grades in a way that allows anyone other than the individual student to access them. Students will be notified by written notice at the time of an assignment if copies of students work will be retained beyond the end of the semester or used as examples for future students or the wider public.

Learner-Centered Elements

Students are responsible for knowing the material in the syllabus section. The Syllabus has important notices and details about the course. Students are responsible for reading the course syllabus and course materials. Most of students' questions will be answered by reviewing the material on the course site in the syllabus section, and by asking questions in class as the course goes on.